What is Claimed is:

1. In a processing system having an unprotected pipeline, an apparatus comprising:

a first logic gate for providing a first signal when a halt signal and a non-interruptible code signal occur together, and

a memory unit for storing the first signal, the first signal indicating a non-returnable interruption of the executing procedure.

2. The apparatus as recited in claim 1 wherein the firs signal is transferred to a read bus.

3. The apparatus as recited in claim 1 wherein the memory unit is a memory-mapped register location.

4. The apparatus as recited in claim 1 wherein the first logic gate is a logic AND gate.

5. The apparatus as recited in claim 1 further comprising:

a second logic, and

a memory unit, the second logic gate providing a halt signal when a trigger signal is applied to a first input terminal and the contents of the memory unit are applied to a second input terminal.

6. A method for transferring a halt signal when a halt signal occurs during a non-interruptible portion of the executing code of a processor having a non-protected pipeline, the method comprising:

determining when a halt signal occurs during a non-interruptible portion of the executing code, and

storing a non-returnable bit in a memory location accessible to testing device.

7. The method as recited in claim 6 wherein, when the control signal is applied to the memory location, applying the non-returnable bit to a read bus.

8. The method as recited in claim 7 wherein the memory unit is a memory-mapped register.

9. A data processing unit comprising:

a processor, the processor including:

a non-protected pipeline,

the processor executing interruptible code and non-interruptible code;

an event signal generating unit, the event signal generating unit generating an event signal in response to a halt condition;

a logic unit responsive to the halt condition and a control signal for generating a halt trigger signal during a non-interruptible code portion; and

a storage unit for storing a non-returnable bit in response to the trigger halt signal.

10. The processing unit as recited in claim 9 wherein the storage unit is a memory-mapped register, the memory mapped register responsive to a control signal for transferring the non-returnable bit outside of the processor.

11. The processing unit as recited in claim 10 further including a storage unit, the storage unit storing an first signal when the processing unit is executing non-interruptible code, the firs signal stored in the storage unit providing the control signal.